1. A method of forming at least one magnetic random access memory cell structure, said method comprising:

forming a mask layer having a predetermined pattern over an insulating layer, said predetermined pattern including first photoresist areas each formed of a masking material of a predetermined width;

reducing said predetermined width of said first photoresist areas to form second reduced-width photoresist areas;

forming at least one groove in said insulating layer using said second reduced-width photoresist areas as a mask;

forming a conductive layer in said at least one groove; and

forming a first magnetic layer over said conductive layer.

2. The method of claim 1, further comprising forming a second magnetic layer over said first magnetic layer.

3. The method of claim 2, further comprising forming a word line over said second magnetic layer.

4. The method of claim 1, wherein said act of forming said at least one groove further comprises etching said insulating layer.

5. The method of claim 1, wherein said act of reducing said predetermined width includes removing portions of said first photoresist areas by etching said first photoresist areas.

6. The method of claim 5, wherein said etching is a reactive ion etching.

7. The method of claim 1, wherein said act of forming said conductive layer further comprises depositing a conductive material inside said at least one groove and planarizing the upper surface of said insulating layer.

8. The method of claim 7, wherein said conductive material is copper.

9. The method of claim 7 further comprising forming a barrier layer in said at least one groove before depositing said conductive material.

10. The method of claim 7 further comprising forming an adhesion layer in said at least one groove before depositing said conductive material.

11. The method of claim 1, wherein said act of forming said first ferromagnetic layer further comprises the step of forming a first plurality of stacked layers, said first plurality of stacked layers including at least one magnetic material layer.

12. The method of claim 11, wherein said magnetic material layer contains a material selected from the group consisting of tantalum, nickel-iron, tungsten-nitrogen, nickel, cobalt-nickel-iron, iron, and manganese-iron.

13. The method of claim 12, wherein said first plurality of stacked layers comprises layers of tantalum, nickel-iron and manganese-iron.

14. The method of claim 11 further comprising etching said first plurality of stacked layers to have a width which coincides with the width of said conductive layer.

15. The method of claim 2, wherein said act of forming said second magnetic layer further comprises forming a second plurality of stacked layers, said second plurality of stacked layers including at least one magnetic material layer.

16. The method of claim 15, wherein said magnetic material layer includes a material selected from the group consisting of tantalum, nickel-iron, tungsten-nitrogen, nickel, cobalt-nickel-iron, iron, and manganese-iron.

17. The method of claim 16, wherein said second plurality of stacked layers comprises layers of tantalum, nickel-iron and tungsten-nitrogen.

18. The method of claim 15 further comprising etching said second plurality of stacked layers.

19. The method of claim 2 further comprising forming a nonmagnetic layer between said first and second magnetic layers.

20. The method of claim 19, wherein said nonmagnetic layer is formed of a material selected from the group consisting of aluminum oxide, titanium oxide, magnesium oxide, silicon oxide and aluminum nitride.

21. The method of claim 19, wherein said nonmagnetic layer is formed of aluminum oxide.

22. The method of claim 1, wherein said conductive layer is longer than 2,000 Angstroms.

23. The method of claim 1, wherein said first ferromagnetic layer has a pinned magnetic orientation.

24. The method of claim 1, wherein said second magnetic layer has a free magnetic orientation.

25. A method of forming a plurality of magnetic random access memory cells over an insulating layer of a semiconductor substrate, said method comprising:

forming a photoresist layer defining a predetermined pattern over said insulating layer, said photoresist layer including first photoresist areas having a predetermined width;

reducing said predetermined width of said first photoresist areas to form second reduced-width photoresist areas;

forming a plurality of grooves in said insulating layer using said second reduced-width photoresist areas as a mask;

forming a plurality of bit line conductive layers in said grooves, said bit line conductive layers being spaced apart from each other by less than 0.20μm;

forming a plurality of first magnetic layers over respective bit line conductive layers;

forming a plurality of second magnetic layers spaced along said first magnetic layers; and

forming a plurality of word layers over respective sets of second magnetic layers, said word lines running substantially orthogonal to said first magnetic layers.

26. The method of claim 25, wherein said act of forming said grooves further comprises etching said insulating layer.

27. The method of claim 25, wherein said act of reducing said predetermined width of said first photoresist areas further includes removing portions of said first photoresist areas by etching said first photoresist areas.

28. The method of claim 27, wherein said etching is a reactive ion etching.

29. The method of claim 25, wherein said act of forming said bit line conductive layers further comprises depositing a conductive material inside said grooves.

30. The method of claim 29, wherein said conductive material is copper.

31. The method of claim 29 further comprising forming a barrier layer in said grooves before depositing said conductive material.

32. The method of claim 29 further comprising forming an adhesion layer in said grooves before depositing said conductive material.

33. The method of claim 25, wherein said act of forming said first magnetic layers further comprises forming a first plurality of stacked layers, said first plurality of stacked layers including at least one magnetic material.

34. The method of claim 33, wherein said magnetic material is selected from the group consisting of tantalum, nickel-iron, tungsten-nitrogen, nickel, cobalt-nickel-iron, iron, and manganese-iron.

35. The method of claim 34, wherein said first plurality of stacked layers comprises layers of tantalum, nickel-iron and manganese-iron.

36. The method of claim 33 further comprising etching said first plurality of stacked layers so that said stacked layers are spaced apart from each other by less than 0.20 μm.

37. The method of claim 25, wherein said act of forming said plurality of second magnetic layers further comprises forming a second plurality of stacked layers, said second plurality of stacked layers including at least one magnetic material.

38. The method of claim 37, wherein said magnetic material is selected from the group consisting of tantalum, nickel-iron, tungsten-nitrogen, nickel, cobalt-nickel-iron, iron, and manganese-iron.

39. The method of claim 38, wherein said second plurality of stacked layers comprises layers of tantalum, nickel-iron and tungsten-nitrogen.

40. The method of claim 25 further comprising forming a nonmagnetic layer between said plurality of first magnetic layers and said plurality of second magnetic layers.

41. The method of claim 40, wherein said nonmagnetic layer is formed of a material selected from the group consisting of aluminum oxide, titanium oxide, magnesium oxide, silicon oxide and aluminum nitride.

42. The method of claim 40, wherein said nonmagnetic layer is formed of aluminum oxide.

43. The method of claim 25, wherein said bit line conductive layers are spaced apart by a distance less than or equal to about 0.1 μm.

44. The method of claim 25, wherein said bit line conductive layers are spaced apart by a distance less than or equal to about 0.05 μm.

45. The method of claim 25, wherein said first magnetic layers have a pinned magnetic orientation.

46. The method of claim 25, wherein a said second magnetic layers have a free magnetic orientation.

47. A magnetic random access memory structure comprising:

a plurality of longitudinally extending conductive bit lines formed over an insulating layer of a semiconductor substrate, said plurality of bit lines being spaced apart from each other by a distance of less than about 0.20μm; and

respective first magnetic layers over said conductive bit lines.

48. The magnetic random access memory structure of claim 47 further comprising a plurality of spaced apart second magnetic layers formed over said plurality of first magnetic layers.

49. The magnetic random access memory structure of claim 48 further comprising a nonmagnetic layer between said plurality of first magnetic layers and said plurality of second magnetic layers.

50. The magnetic random access memory structure of claim 49, wherein said nonmagnetic layer comprises a material selected from the group consisting of aluminum oxide, titanium oxide, magnesium oxide, silicon oxide and aluminum nitride.

51. The magnetic random access memory structure of claim 49, wherein said nonmagnetic layer comprises aluminum oxide.

52. The magnetic random access memory structure of claim 47 further comprising a barrier layer formed between said bit lines and said insulating layer.

53. The magnetic random access memory structure of claim 47, wherein each said first magnetic layer includes a magnetic material selected from the group consisting of tantalum, nickel-iron, tungsten-nitrogen, nickel, cobalt-nickel-iron, iron, and manganese-iron.

54. The magnetic random access memory structure of claim 48, wherein each said second magnetic layer includes a ferromagnetic material selected from the group consisting of tantalum, nickel-iron, tungsten-nitrogen, nickel, cobalt-nickel-iron, iron, and manganese-iron.

55. The magnetic random access memory structure of claim 47, wherein said bit lines are longer than 2,000 Angstroms.

56. The magnetic random access memory structure of claim 47, wherein said bit lines are spaced apart by a distance of less than or equal to about 0.1 μm.

57. The magnetic random access memory structure of claim 47, wherein said bit lines are spaced apart by a distance of less than or equal to about 0.05 μm.

58. The magnetic random access memory structure of claim 47, wherein said first magnetic layers have a pinned magnetic orientation.

59. The magnetic random access memory structure of claim 48, wherein said second magnetic layers have a free magnetic orientation.

60. A memory device comprising:

at least one magnetic random access memory cell, said magnetic random access memory cell comprising a first ferromagnetic layer formed over a bit line conductor, a second ferromagnetic layer formed over said first ferromagnetic layer, a nonmagnetic layer between said first and second ferromagnetic layers, and a word line in contact with said second ferromagnetic layer, said memory cell being arranged so that said bit line conductor is spaced from an adjacent bit line conductor by a distance of less than or equal to about 0.20 μm.

61. The memory device of claim 60, wherein said bit line conductor is spaced from an adjacent bit line conductor by a distance of less than or equal to about 0.1 μm.

62. The memory device of claim 60, wherein said bit line conductor is spaced from an adjacent bit line conductor by a distance of less than or equal to about 0.05 μm.

63. The memory device of claim 60, wherein said bit line conductor is longer than 2,000 Angstroms.

64. The memory device of claim 60, wherein said first ferromagnetic layer has a pinned magnetic orientation.

65. The memory device of claim 60, wherein said second ferromagnetic layer has a free magnetic orientation.

66. A processor-based system, comprising:

a processor; and

an integrated circuit coupled to said processor, said integrated circuit including a plurality of magnetic random access memory cells, each of said magnetic random access memory cells including a first ferromagnetic layer formed over a bit line conductor, a second ferromagnetic layer formed over said first ferromagnetic layer, a nonmagnetic layer between said first and second ferromagnetic layers, and a word line

in contact with said second ferromagnetic layer, said memory cell being arranged so that said bit line conductor is spaced from an adjacent bit line conductor by a distance less than or equal to about 0.25 μm.

67. The processor-based system of claim 66, wherein said bit line conductor is spaced from an adjacent bit line conductor by a distance of less than or equal to about 0.1 μm.

68. The processor-based system of claim 66, wherein said bit line conductor is spaced from an adjacent bit line conductor by a distance of less than or equal to about 0.05 μm.

69. The processor-based system of claim 66, wherein said nonmagnetic layer comprises a material selected from the group consisting of aluminum oxide, titanium oxide, magnesium oxide, silicon oxide and aluminum nitride.

70. The processor-based system of claim 66, wherein said bit line conductor is longer than 2,000 Angstroms.

71. The processor-based system of claim 66, wherein said first ferromagnetic layer has a pinned magnetic orientation.

72. The processor-based system of claim 66, wherein said second ferromagnetic layer has a free magnetic orientation.